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10/661,225	09/12/2003	Huy Nguyen	60809-0132-US	6839

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/661,225	NGUYEN ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09-12-03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 05-02-07. Applicant's arguments with 35 U.S.C. 112,2nd problem and the prior art of reference have been carefully considered but they are not deemed to be persuasive. Thus, the claims remained rejected under 35 U.S.C. 112,2nd. and under Desai. However, the rejection changes slightly for clarification.

Specification

The disclosure is objected to because of the following informalities: the disclosure "In alternate embodiments, duty cycle detector 228 includes or is coupled to a comparator that determines the difference between the data signal duty cycle and the predetermined duty cycle. The skew values (i.e., SkA, SkB) are then based on this difference" on page 8, 2nd paragraph is misleading because there is no "predetermined duty cycle" signal input to circuit (228) so that circuit (228) can compare the "data duty cycle" and the "predetermined duty cycle" to determine the difference between the data signal duty cycle and the predetermined cycle. Note that circuit (228) shows only one input signal (226).

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first correction circuit" in claim 21 and the "second correction circuit" in claim 27 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be

necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 6 and 27 is objected to because of the following informalities: the recitation "The integrated circuit of claim 21, including a clock duty cycle detector configured to detect a duty cycle of the system clock signal and to generate a third difference signal representing a difference between the detected system clock signal duty cycle and the first predetermined duty cycle; and a second correction circuit configured to adjust the duty cycle of the receiver clock signal in accordance with the third difference signal" is confusing because it is not clear what the "a third difference signal" is and how it is generated the detected system clock signal duty cycle and the first predetermined duty cycle. No drawing shows a second correction configured to adjust the duty cycle of the receiver clock signal in accordance with the third difference signal. Dependent claims 7-11 and 28-32 carry over any objection from claim 27 which they depend.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and /or clarification is required.

Regarding claim 1, the recitation "detecting a duty cycle of a data signal; comparing the detected duty cycle with a predetermined duty cycle in order to determine a first difference between the detected data signal duty cycle and the predetermined duty cycle"

is indefinite because it is misdescriptive. Figure 2B of the present application shows that when the data (226) is detected and the circuit of figure 2B generates two skew values (SkA, SkB). In figure 2C, comparator (242) compares the data signal (226) with the "a predetermined duty cycle" assumed to be the output of circuit (240) to produce a difference of these two signals. It is clear that the data signal (226) is not the "detected duty cycle" or the "the detected data signal duty cycle" that is compared with "predetermined duty cycle". There is no indication that "detected duty cycle" or the "the detected data signal duty cycle" of data signal (226) is compared with "a predetermined duty cycle" in the circuit of figure 2C. In fact, the data signal (226) is directly compared with the "a predetermined duty cycle" by circuit (242). It is not clear as to the " detected duty cycle" on line 4 is same or different than the detected "duty cycle of a data signal" on line 3. The Applicant is requested to clarify what the "a data signal", the "detected duty cycle", "the detected data signal duty cycle", "a receiver clock" and the "a predetermined duty cycle" are. The recitation "the detected data signal duty cycle" on line 5 is indefinite because it is not clear as to this "the detected data signal duty cycle" is the same or different than "the detected duty cycle" on line 4. The recitations "the detected data signal duty cycle" and "the detected duty cycle" lack antecedent basis. The recitation "adjusting a duty cycle of the receiver clock in accordance with the first difference between the detected data signal duty cycle and the predetermined duty cycle" has the same 112, 2nd problem above. The Applicant is requested to show the "a duty cycle of the receiver clock" and the "detected data signal duty cycle" in the drawing.

Regarding claim 2, the recitation "the step of comparing the detected duty cycle with a predetermined duty cycle comprises comparing the first duty cycle with a first predetermined duty cycle in order to determine a first difference between the first duty cycle and the first predetermined duty cycle, and comparing the second duty cycle with a second predetermined duty cycle in order to determine a second difference between the second duty cycle and the second predetermined duty cycle" is confusing because it is not clear as to "the first duty cycle" and the "the second duty cycle" are the same or different than "the detected duty cycle". They are all compared with the "a predetermined duty cycle".

Regarding claim 6, the recitation "comparing the duty cycle of the system clock signal with the predetermined duty cycle" is indefinite because it is confusing. In the Remarks

the Applicant admits that the " predetermined duty cycle" is the same as the "predetermined duty cycle" in claim 1. In claim 1, the "predetermined duty cycle" is compared with the "detected duty cycle" which is the detected duty cycle of the data signal is compared with the "predetermined duty cycle". Thus, claim 6 is misdescriptive because the "predetermined duty cycle" is compared with two different signals related to the data signal and the system clock signal. Figure 2C shows that comparator (242) only compares the data signal and the "predetermined duty cycle" that is assumed to be the output of circuit (240). For clarification, the Applicant is requested to point out in the drawing the "detected duty cycle" in claim 1, the "duty cycle of the system clock signal" and the "predetermined duty cycle" in claim 6.

Regarding claim 21, the recitation " data signal duty cycle detector configured to detect a first duty cycle of a first data signal and to generate a first difference signal representing a difference between the first duty cycle and a first predetermined duty cycle" is indefinite because it is misdescriptive. Figure 2B of the present application shows that the "data signal duty cycle detector" (the duty cycle detector 228) does not generates "a first difference signal" as recited. Figure 2B shows that the duty cycle detector (228) generates signals (SkA, SkB) that are not the "a first difference signal". Figure 2C of the present application shows that comparator (242) generates "the first different signal". Clear clarification is required.

Claims 3-5, 7-20 and 22-41 are indefinite because of the technical deficiencies of claim 1 and 21

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 21-26 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Desai (US. 6,862,296).

Regarding claims 1-4, figure 5 of Desai shows a method of adjusting a receiver clock duty cycle, comprising:

receiving a system clock signal (Recovered clock);

detecting a duty cycle of a data signal and comparing the detected duty cycle with a predetermined duty cycle (Reference Pattern) in order to determine a first difference (Match) between the detected data signal duty cycle and the predetermined duty cycle;

generating (506) a receiver clock (Word Clock) from the system clock signal (Recovered clock); and

adjusting a duty cycle of the receiver clock in accordance with the first difference (Match) between the detected data signal duty cycle and the predetermined duty cycle. Comparator (508) compares the detected duty cycle with a predetermined duty cycle (Reference Pattern) and generates the first difference (Match).

Regarding claims 2-4, figure 5 of Desai shows that the output of element (504) contains eight different duty cycles that are then compared with eight different predetermined duty cycles (Reference Pattern). Thus, figure 5 of Desai fully shows all the limitations of claims 2-4.

Regarding claims 21, figure 5 of Desai shows an integrated circuit, comprising:

a clock receiver (502, 504) configured to receive a system clock signal (Recovered Clock) having a duty cycle;

a data signal duty cycle detector (508, 500) configured to detect a first duty cycle of a first data signal and to generate a first difference signal (Match) representing a difference between the first duty cycle and a first predetermined duty cycle (Reference Pattern); and

a receiver clock generator (506) configured to output a receiver clock signal (Word Clock) based on the system clock signal (Recovered Clock) and the first different signal (Match), the receiver clock generator including a first correction circuit, not shown, configured to adjust a duty cycle of the receiver clock signal (Word Clock) in accordance with the first difference signal (Match).

Regarding claim 22, the data signal duty cycle detector (508, 500) receives eight data signals (including a second data signal) and generates a second difference signal (Match). The receiver clock generator (506) is configured to output a first receiver clock signal (Word Clock) based on the system clock signal (Recovered Clock) and the first difference signal (Match).

Regarding claims 23-26. The output of element (504) presents a plurality (8) of different data signals. And there is a plurality (8) of predetermined duty cycles (Reference Pattern). Inherently, the data signals can be generated from different devices located on different ICs and the predetermined duty cycle can be adjusted as required. Also, because there are a plurality of data and predetermined duty cycles, there is a plurality of difference signals, including a third on in claim 27.

Regarding claim 42 figure 5 of Desai shows an integrated circuit, comprising: an integrated circuit, comprising:

means for receiving a system clock signal (506) having a duty cycle; means for detecting a duty cycle of a data signal (508) and for generating a first difference signal (Shift) representing a difference between the detected data signal duty cycle and a predetermined duty cycle; and

means for generating a receiver clock signal (506) based on the system clock signal and the first difference signal, including means (500) for adjusting a duty cycle of the receiver clock signal in accordance with the first difference signal.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 13, 14, 18-20, 34, 35 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Desai (US. 6,862,296).

Regarding claims 5, 13, 14,18-20, 25, 26 and 39-41 figure 5 of Desai includes all the limitations of these claims except for different values of the duty cycles, the devices that generate data signals, first and second device that can be located on different ICs and the difference and the sources of the data signal. However, it is well known to one of ordinary skill in the art that first difference can be set to desired value and the data signals can be provided from different ICs and the first and second device can be located on different ICs can be adjusted to proper duty cycles.

Response to Arguments

According to the Remarks page 10, last paragraph, the Applicant alleges that the "a data signal duty cycle detector" is the "duty cycle detector 228 in figure 2B". This is not correct because circuit 228 in figure 2B generates signals (SkA, SkB). Signals (SkA) or (SkB) is not "a first difference signal representing a difference between the first duty cycle and the first predetermined duty cycle". Figure 2B does not show "the first predetermined duty cycle" connected to circuit (228). To clarify the ambiguity of the claim, the Applicant is requested to show the "first duty cycle" and the "first predetermined duty cycle" that are connected to circuit (228).

On page 11, the Applicant argues that " it is noted that Desai's comparator 508 does not detect and compare duty cycles. In fact, the comparator 508 cannot receive any information concerning the duty cycle of the received serial data, because the sampling flip-flop 502 "retimes the serial data". The Applicant is reminded that the claims are rejected based on the broadest reasonable interpretation of the claimed limitations and the prior art reference(s). Claim 1 recites: "detecting a duty cycle of a data signal". One of ordinary skill in the art would understand that every signal has a duty cycle comprising a high level. Element (502) of Desai detects the high level of the data signal (serial data) and provides an output signal that reflexes the high level (and the low level) of the data signal. Thus, according to the broadest reasonable interpretation of the claimed limitations, element (502) is a duty cycle detector. The output(s) of element (504) contains the detected duty cycle of the data signal, the detected duty cycle, is compared with a predetermined duty cycle (Reference Pattern) and the output of the comparator (508) provide the difference between the detected data signal and

the predetermined duty cycle. Element (506) generates the receiver clock (Word Clock) from the system clock signal (Recovered Clock) and the duty cycle of the receiver clock is adjusted in accordance with the first difference (Match) between the detected data duty cycle and the predetermined duty cycle. In claim 1, the Applicant is silent about the process of detecting a duty cycle of a data signal. Thus, with the broadest reasonable interpretation of the claimed limitations any circuit that detects a high level of a signal and outputs a corresponding high level signal is considered to be a duty cycle detector. In conclusion, the limitations of claim 1 are fully read on figure 5 of Desai.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
07-03-07

TUAN T. LAM
PRIMARY EXAMINER